|  | **Pimpri Chinchwad Education Trust’s**  **Pimpri Chinchwad College of Engineering** |
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| **Experiment 6**  **Experimentation details** | |

**Department: E&TC Academic Year: 2023-24 Semester-I**

**Class: B.Tech E&TC Course: VLSI Design Lab**

**Name of Student:**

**Div and Batch: A,A1**

**Roll No:**

**Title of the Experiment:**

**Model and verify 4-bit Universal shift using VHDL and implement on FPGA and evaluate power and timing performance**

**Software Requirements: Xilinx 14.7 ISE Design Suite**

**Hardware Requirements: Xilinx Spartan-6 XC6SLX45 FPGA**

**VHDL Code for Simulation**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_arith.ALL;

use IEEE.STD\_LOGIC\_unsigned.ALL;

entity usr is

Port ( Clk,rst,sin : in STD\_LOGIC;

m : in STD\_LOGIC\_VECTOR (1 downto 0);

pin : in STD\_LOGIC\_VECTOR (3 downto 0);

sout : out STD\_LOGIC;

pout : out STD\_LOGIC\_VECTOR (3 downto 0));

end usr;

architecture Behavioral of usr is

signal p1,p2:std\_logic\_vector(3 downto 0);

signal s1:std\_logic;

begin

process(clk,rst,pin,sin,m)

begin

if(rst='1') then

p1<="0000";

p2<="0000";

s1<='0';

elsif (clk'event and clk='1') then

if(m="00") then --SISO

p1(0)<=sin;

p1(1)<=p1(0);

p1(2)<=p1(1);

p1(3)<=p1(2);

s1<=p1(3);

elsif(m="01") then --SIPO

p1(0)<=sin;

p1(1)<=p1(0);

p1(2)<=p1(1);

p1(3)<=p1(2);

p2<=p1;

elsif(m="10") then --PIPO

p1<=pin;

p2<=p1;

else --PISO

p1<=pin;

s1<=p1(3);

end if;

end if;

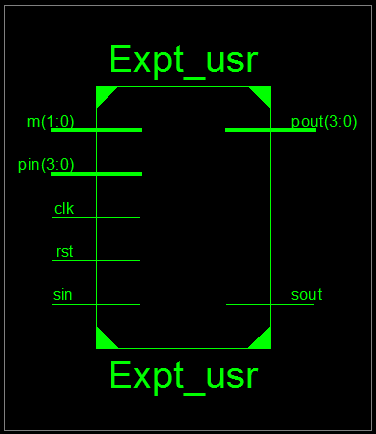
end process;

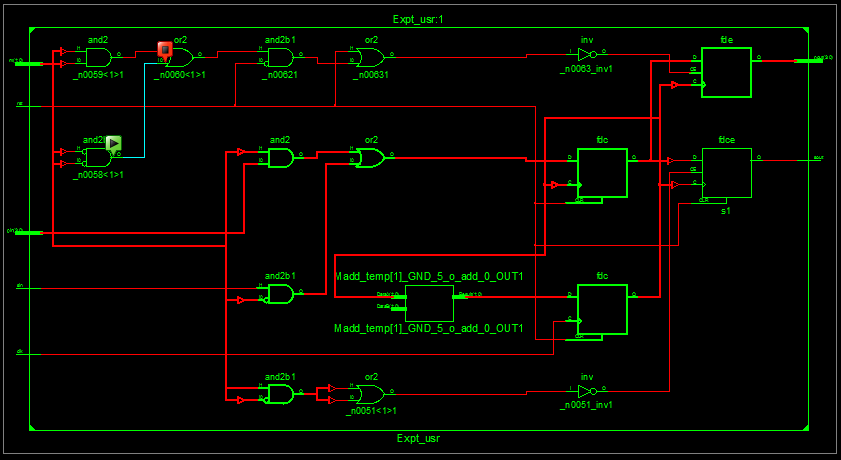
pout<=p2;

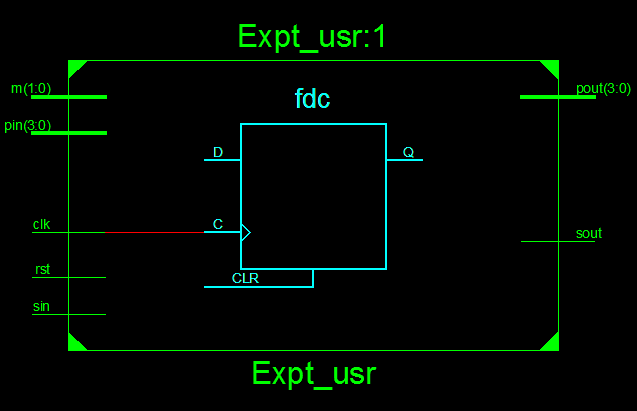
sout<=s1;

end Behavioral;

**RTL Schematic**

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**VHDL Test Bench**

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric\_std.ALL;

ENTITY usr\_tb IS

END usr\_tb;

ARCHITECTURE behavior OF usr\_tb IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT usr

PORT(

Clk : IN std\_logic;

rst : IN std\_logic;

sin : IN std\_logic;

m : IN std\_logic\_vector(1 downto 0);

pin : IN std\_logic\_vector(3 downto 0);

sout : OUT std\_logic;

pout : OUT std\_logic\_vector(3 downto 0)

);

END COMPONENT;

--Inputs

signal Clk : std\_logic := '0';

signal rst : std\_logic := '0';

signal sin : std\_logic := '0';

signal m : std\_logic\_vector(1 downto 0) := (others => '0');

signal pin : std\_logic\_vector(3 downto 0) := (others => '0');

--Outputs

signal sout : std\_logic;

signal pout : std\_logic\_vector(3 downto 0);

-- Clock period definitions

constant Clk\_period : time := 20 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: usr PORT MAP (

Clk => Clk,

rst => rst,

sin => sin,

m => m,

pin => pin,

sout => sout,

pout => pout

);

-- Clock process definitions

Clk\_process :process

begin

Clk <= '0';

wait for Clk\_period/2;

Clk <= '1';

wait for Clk\_period/2;

end process;

rst\_process :process

begin

rst <= '1';

wait for Clk\_period;

rst <= '0';

wait;

end process;

-- Stimulus process

stim\_proc: process

begin

pin<="1001";

sin<='1';

m<="00”; -- SISO

wait for 120 ns;

pin<="1101";

sin<='1';

m<="01"; -- SIPO

wait for 120 ns;

pin<="1101"; --PIPO

m<="10";

wait for 120 ns;

pin<="0100"; -- PISO

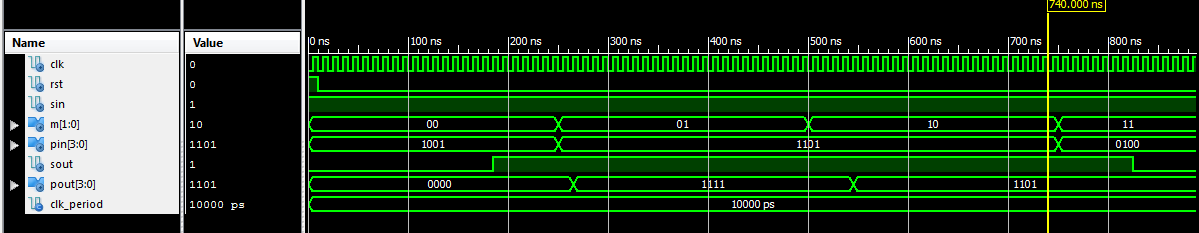
m<="11";

wait;

end process;

END;

**Simulation Results**



**VHDL Code for Implementation**

**Plz note:**

**1. Clock freq of board= 8MhZ. So, a process is added to generate a slow clock of freq = 1 Hz**

**2. for slowing down the clk from 8 MHz to 1 Khz, a temp counter of size 23 bits is**

**introduced for generating delay**

**VHDL Code:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_arith.ALL;

use IEEE.STD\_LOGIC\_unsigned.ALL;

entity usr is

Port ( Clk,rst,sin : in STD\_LOGIC;

m : in STD\_LOGIC\_VECTOR (1 downto 0);

pin : in STD\_LOGIC\_VECTOR (3 downto 0);

sout : out STD\_LOGIC;

pout : out STD\_LOGIC\_VECTOR (3 downto 0));

end usr;

architecture Behavioral of usr is

signal p1,p2:std\_logic\_vector(3 downto 0);

signal s1:std\_logic;

**signal temp:std\_logic\_vector(22 downto 0);**

**signal sclk:std\_logic;**

begin

**p11: process(clk,rst)**

**begin**

**if(rst='1')then temp<=(others=>'0');**

**elsif(clk'event and clk='1') then**

**temp<= temp + 1;**

**end if;**

**end process;**

**sclk<=temp(22);**

p22:process(sclk,rst,pin,sin,m)

begin

if(rst='1') then

p1<="0000";

p2<="0000";

s1<='0';

elsif (sclk'event and sclk='1') then

if(m="00") then --SISO

p1(0)<=sin;

p1(1)<=p1(0);

p1(2)<=p1(1);

p1(3)<=p1(2);

s1<=p1(3);

elsif (m="01") then --SIPO

p1(0)<=sin;

p1(1)<=p1(0);

p1(2)<=p1(1);

p1(3)<=p1(2);

p2<=p1;

elsif(m="10") then --PIPO

p1<=pin;

p2<=p1;

else --PISO

p1<=pin;

s1<=p1(3);

end if;

end if;

end process;

pout<=p2;

sout<=s1;

end Behavioral;

**Implementation Constraint File (UCF File)**

NET "CLK" LOC = "L15"; # Bank = 1, Pin name = IO\_L42P\_GCLK7\_M1UDM, Type = GCLK, Sch name = GCLK

**# onBoardLeds**

NET "pout<0>" LOC = "U18"; # Bank = 1, Pin name = IO\_L52N\_M1DQ15, Sch name = LD0

NET "pout<1>" LOC = "M14"; # Bank = 1, Pin name = IO\_L53P, Sch name = LD1

NET "pout<2>" LOC = "N14"; # Bank = 1, Pin name = IO\_L53N\_VREF, Sch name = LD2

NET "pout<3>" LOC = "L14"; # Bank = 1, Pin name = IO\_L61P, Sch name = LD3

NET "Sout" LOC = "M13"; # Bank = 1, Pin name = IO\_L61N, Sch name = LD4

**# onBoard SWITCHES**

NET "pin<0>" LOC = "A10"; # Bank = 0, Pin name = IO\_L37N\_GCLK12, Sch name = SW0

NET "pin<1>" LOC = "D14"; # Bank = 0, Pin name = IO\_L65P\_SCP3, Sch name = SW1

NET "pin<2>" LOC = "C14"; # Bank = 0, Pin name = IO\_L65N\_SCP2, Sch name = SW2

NET "pin<3>" LOC = "P15"; # Bank = 1, Pin name = IO\_L74P\_AWAKE\_1, Sch name = SW3

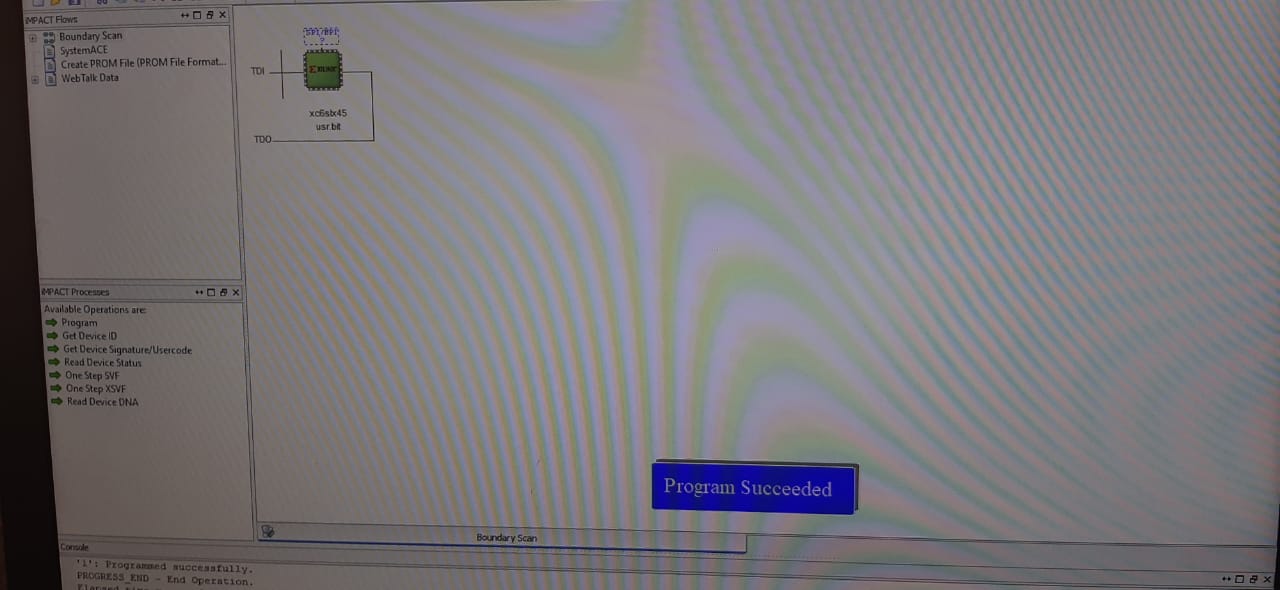
NET "sin" LOC = "P12"; # Bank = 2, Pin name = IO\_L13N\_D10, Sch name = SW4

NET "rst" LOC = "R5"; # Bank = 2, Pin name = IO\_L48P\_D7, Sch name = SW5

NET "m<0>" LOC = "T5"; # Bank = 2, Pin name = IO\_L48N\_RDWR\_B\_VREF\_2, Sch name = SW6

NET "m<1>" LOC = "E4"; # Bank = 3, Pin name = IO\_L54P\_M3RESET, Sch name = SW7

**Implementation Successful**



**Hardware Snapshots**

**Digilent ATLYS Spartan 6 FPGA Board**

